1. (amended) A method of operating a multi-level cache of a computer system, comprising the steps of:

monitoring cache activity of an upper level cache and a lower level cache both associated with a processor of the computer system, said monitoring including monitoring cache hits in the upper level cache;

issuing a request from the processor to load a value, wherein the request misses the upper level cache and the lower level cache; and

selecting a victim cache block in the lower level cache for receiving the requested value based at least in part on cache hits in the upper level cache.

2. (unchanged) The method of Claim 1 wherein the victim cache block is further selected based in part on the cache activity of the lower level cache.

3. (unchanged) The method of Claim 1 wherein said selecting step takes place out of a critical path of execution of a core of the processor.

4. (unchanged) The method of Claim 1 wherein said issuing step issues a request to load operand data.

5. (unchanged) The method of Claim 1 wherein said selecting step includes the step of identifying a less recently used cache block in the lower level cache.

6. (unchanged) The method of Claim 1 further comprising the steps of:

returning the requested value to the processor;

determining that it would be efficient to currently load into the upper level cache a cache line which includes the requested value; and

in response to said determining step, loading the cache line into the upper level cache.

7. (unchanged) The method of Claim 1 wherein:

said monitoring step monitors cache misses of the upper level and lower level caches; and

said selecting step selects the victim cache block based at least in part on the cache misses of the lower level cache.

Cancel claims 8-9

10. (amended) The method of Claim 1 further comprising the step of selecting a victim cache block in the upper level cache for receiving the requested value based at least in part on the cache activity of the lower level cache.

11. (amended) A computer system comprising:

a system memory device;

means for processing program instructions;

means, connected to said processing means, for caching values stored in said system memory device, said caching means having at least an upper level cache and a lower level cache both associated with said processing means;

means for monitoring cache activity of said upper level cache and said lower level cache including cache hits in the upper level cache; and

means for selecting a victim cache block in said lower level cache for receiving a value

specified in a load request issued by said processing means, wherein the load request missed said upper level cache and said lower level cache, based at least in part on cache hits in said upper level cache.

12. (unchanged) The computer system of Claim 11 wherein said selecting means is located out of a critical path of execution of a core of said processing means.

13. (unchanged) The computer system of Claim 11 wherein said upper level cache is an operand data cache.

14. (unchanged) The computer system of Claim 11 wherein said selecting means identifies a less recently used cache block in said upper level cache.

15. (unchanged) The computer system of Claim 11 wherein:

said upper level cache is an L1 cache; and

said lower level cache is an L2 cache.

16. (unchanged) The computer system of Claim 11 wherein said upper level cache is a store-through cache.

17. (unchanged) The computer system of Claim 11 further comprising:

means for returning the requested value to said processing means in response to the load request missing said upper level cache; and

means for loading a cache line which includes the requested value into said upper level cache in response to a determination that it would be efficient to currently load the cache line into said upper level cache.

18. (unchanged) The computer system of Claim 11 wherein:

said monitoring means monitors cache misses of said lower level cache; and

said selecting means selects said victim cache block based at least in part on the cache misses of said lower level cache.

Cancel claims 19-20

21. (amended) The computer system of Claim 11 further comprising means for selecting a victim cache block in said upper level cache for receiving the requested value based at least in part on the cache activity of said lower level cache.

22. (newly entered) A processing unit, comprising:

at least one instruction execution unit;

at least an upper level cache and a lower level cache;

a cache controller that, responsive to receipt of a load request issued by said at least one execution unit that missed said upper level cache and said lower level cache, selects a victim cache block in said lower level cache for receiving a value specified in the load request, wherein the selection is based at least in part on cache hits in said upper level cache.

23. (newly entered) The processing unit of Claim 22, wherein said upper level cache is an operand data cache.

24. (newly entered) The processing unit of Claim 22, wherein said upper level cache is a store-through cache.

25. (newly entered) The processing unit of Claim 22, further comprising:

means for loading a cache line including the requested value into said upper level cache in response to a determination that it would be efficient to load the cache line into said upper level cache.

26. (newly entered) The processing unit of Claim 22, wherein said cache controller selects said victim cache block based at least in part on the cache misses of said lower level cache.

27. (newly entered) The processing unit of Claim 22, and further comprising means for selecting a victim cache block in said upper level cache for receiving the requested value based at least in part on the cache activity of said lower level cache.